Large area interline CCD with low dark current

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Abstract

When interline CCD image sensors increase in size beyond 4 million pixels, CCD dark current begins to degrade the signal. Some scientific and photographic applications use very slow readout rates (less than 1 MHz) to reduce the noise level. At a 1-MHz readout rate, a 4-megapixel imager will take at least 4 s to read out. This extended time period allows a significant amount of dark current to build up and frustrate efforts to reduce noise. Often this situation leads to the additional expense of a low-temperature operation. The accumulation-mode readout method for interline CCD image sensors is being developed at Eastman Kodak Company. Previously, accumulation mode could only be applied to the full-frame architecture because the p-type substrate acted as a source for holes. Interline CCD image sensors with n-type substrates have no ready source of holes to accumulate the surface of the CCD under all phases. This problem has been overcome, allowing room-temperature operation without significant dark current generation.

Keywords: interline, CCD, dark current, image sensor, accumulation, noise

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1. INTRODUCTION

This paper about low interline CCD dark current centers around the two large area interline CCDs manufactured by Eastman Kodak Company, the Kodak KAI-4020 image sensor and the Kodak KAI-11000 image sensor. The KAI-4020 is a 4-megapixel image sensor with high output gain (30 μV/e), and the KAI-11000 is an 11-megapixel 35 mm photographic format image sensor. The interline CCD unit pixel consists of a photodiode and a vertical CCD (VCCD) as shown in Figure 1. The photodiode integrates photoelectrons while the VCCD shifts the previously acquired image towards the horizontal CCD and the output amplifier. The full-frame type CCD image sensor does not have separate photodiode sites in each pixel. Instead, the VCCD is exposed to light and occupies the entire pixel area.

An important difference between the interline CCD and full-frame CCD architectures is the substrate type. The full-frame CCD comprises an n-type buried channel in a p-type substrate. The interline CCD also has an n-type buried channel, except the buried channel is built in a p-type well on an n-type substrate. This is illustrated in Figure 1. The n-type substrate is required to construct the vertical overflow drain structure of the photodiode. The full-frame CCD uses an n-type implanted lateral overflow drain structure. How the substrate type is critical to low dark current clocking of a CCD is the subject of this report.

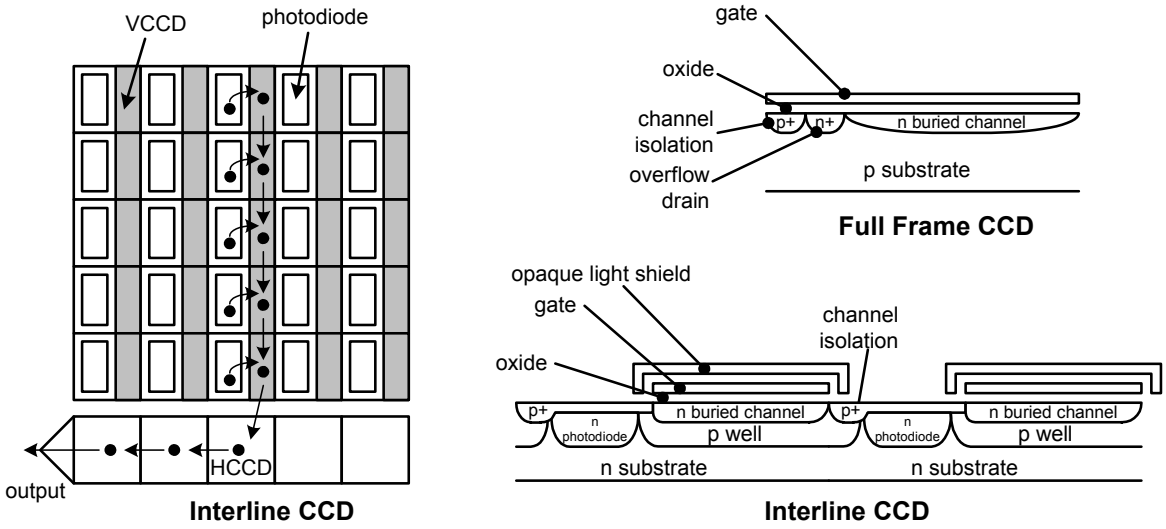

Figure 1: The differences between the full-frame and interline CCD architectures.

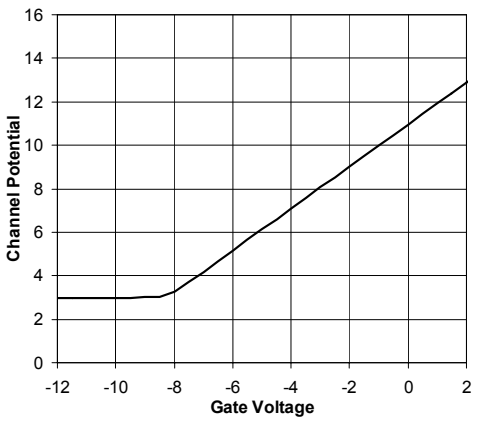

Figure 2: VCCD channel potential vs gate voltage

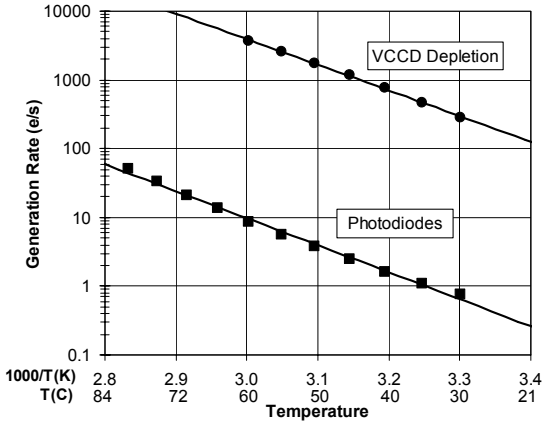

Figure 3: The dark current generation rate (electrons/sec) vs temperature for a line rate of 416 Hz

2. Depletion Mode Dark Current

The charge packets in a CCD are moved along the shift register by clocking the gates of the CCD. Figure 2 shows how the channel potential under a gate depends on the gate voltage. Above –8 V the channel potential has a linear dependence on gate voltage. This is the range of gate voltages where the CCD surface is depleted of holes. Below -8 V, the channel potential is a constant. This is because the potential at the surface reaches 0 V and the p+ channel isolation regions supply holes to the surface of the CCD and pin the potential at 0 V. In this condition the CCD surface is accumulated by holes. The holes recombine with electrons in surface defect levels. This dramatically reduces the surface dark current generation rate compared to when the CCD surface is depleted of holes.[1]

The KAI-4020 sensor is a two-phase CCD. Its depletion mode clocking sequence is shown in Figure 4. Each phase of the VCCD is clocked to –9 V to ensure holes reach the surface of the CCD to keep the depletion mode dark current at a minimum. The temperature dependence of the depletion mode dark current is shown in Figure 3. This data was measured at a pixel frequency of 1 MHz and a line rate of 416 Hz. The dark current data must be given along with the VCCD clocking frequency. This is because the dark current generation rate is dependent on the VCCD clock frequency.[2] When a depleted gate is clocked into accumulation and back to depletion, it takes time for the defect levels to repopulate. Longer line times allow more defect levels to repopulate, which increases the dark current. Figure 5 shows the dark current generation rate dependence on the VCCD clock period (line time).

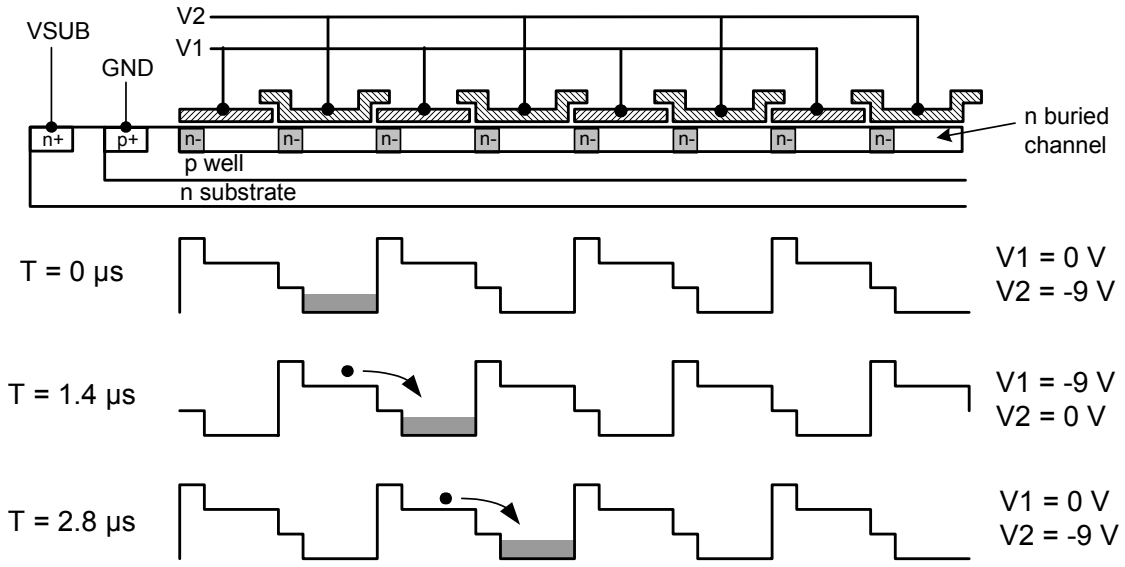

Figure 4: The depletion mode clocking sequence.

Now consider the case of an image acquired from the KAI-4020 sensor at a readout frequency of 1 MHz and temperature of 40 C. The total time to read out the image sensor is 5 s. If electronic shuttering is not used then the exposure time will also be 5 s. From Figure 3 the average photodiode dark current, will be 8 electrons. The noise component from the photodiode dark current will be 2.8 electrons. The problem is in the dark current signal added while image is being shifted through the VCCD, 3800 electrons. This noise component from the VCCD dark current will be 195 electrons. The VCCD dark current noise dominates and makes the slow readout rate useless for obtaining a low noise image. Even if the readout rate is

increased to 30 MHz, the VCCD dark current noise will still contribute approximately 15 electrons noise to the image on the 11 megapixel KAI-11000 sensor interline CCD.

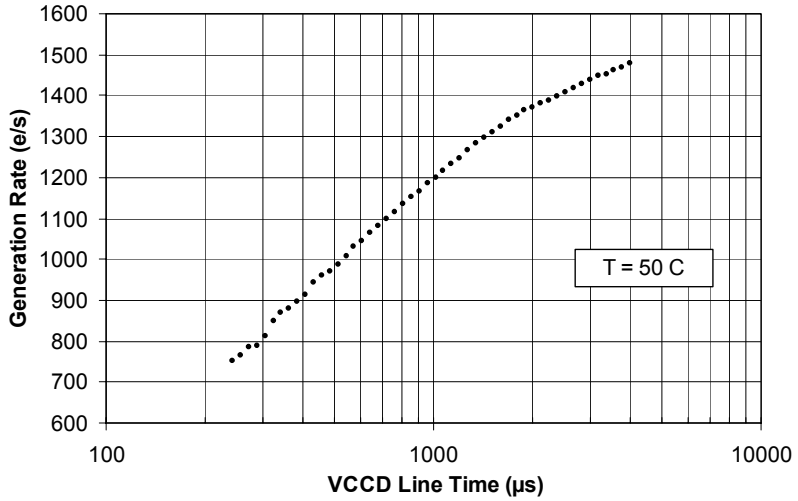

Figure 5: The VCCD dark current generation rate vs. the VCCD clock period at T = 50ºC.

This presents a problem for the development of large interline CCDs for digital photography. Cooling the image sensor is not an option in a portable digital camera. Depending on the environment, the internal camera temperature could reach 50 C. If large interline CCDs are to be used in digital photography, reduced VCCD dark current is critical.

3. ACCUMULATION MODE DARK CURRENT

Accumulation mode clocking of the VCCD is a well-known method to reduce dark current on full-frame image sensors.[1] However, applying standard accumulation mode clocking to an interline CCD results in poor charge transfer efficiency (CTE). By increasing charge transfer times to compensate, the dark current increases enough to make accumulation mode clocking produce only a minor decrease of dark current. The poor CTE is due to the interline CCD being built in a p-type well on an n-type substrate. To understand this, first consider the accumulation mode timing sequence shown in Figure 6 and the timing diagram of Figure 7.

In accumulation mode both gates are held in accumulation at –9 V while the horizontal CCD is being clocked to the output amplifier. In depletion mode only one gate is held at –9 V, the other gate is held in depletion at 0 V. It is the gate held in depletion that generates all of the objectionable dark current. In the accumulation mode timing sequence of Figure 7, each gate is separately clocked into depletion for a short time period to shift the charge packet by one pixel. This accumulation mode timing sequence works well on full-frame image sensors because the p-type substrate acts as a ready source of holes to accumulate the surface. The resistance to the flow of holes from the substrate ground connection in Figure 6 is low. In the interline CCD structure shown in Figure 4, the ground contact must be made to the p-well at the end of the VCCD. There is a very long, highly resistive (MΩ), path for holes from the end of the VCCD to the center. At the accumulation mode clock transition of V1 in Figure 7 between times T1 and T2, there is no clock transition on V2. This is the source of the charge transfer problems. When the V1 gate transitions from –9 V to 0 V no holes will be able to leave the center of the VCCD in a reasonable amount of time. The capacitive coupling of the V1 gate to the p-well 'drags' the p-well voltage away from 0 V (ground) and prevents charge transfer. For a large area 35 mm format CCD it could take as long as 200 µs for the p-well to return to 0 V. Capacitive coupling of the VCCD gates to the p-well is called p-well bounce.

Backside thinned full-frame image sensors may also suffer from unstable substrate voltages. Poor or no electrical contact to the back of the substrate directly under the CCD will result in p-well or p-substrate bounce.

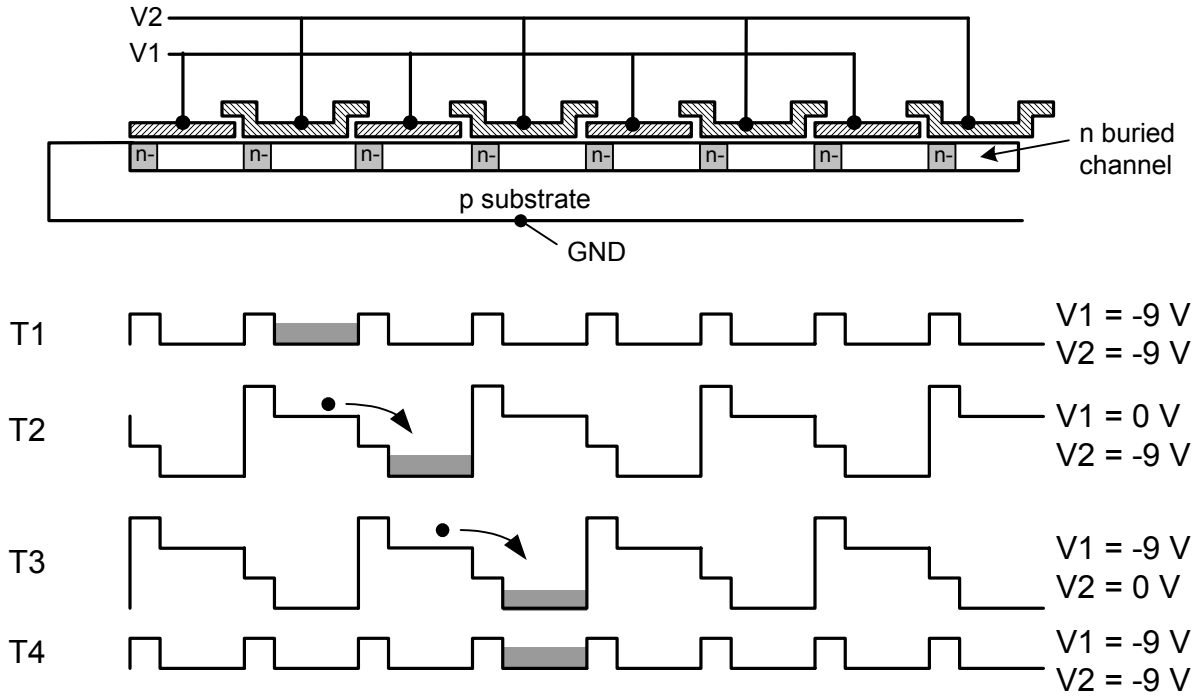

Figure 6: The accumulation mode timing sequence on a full-frame CCD with a p-type substrate.

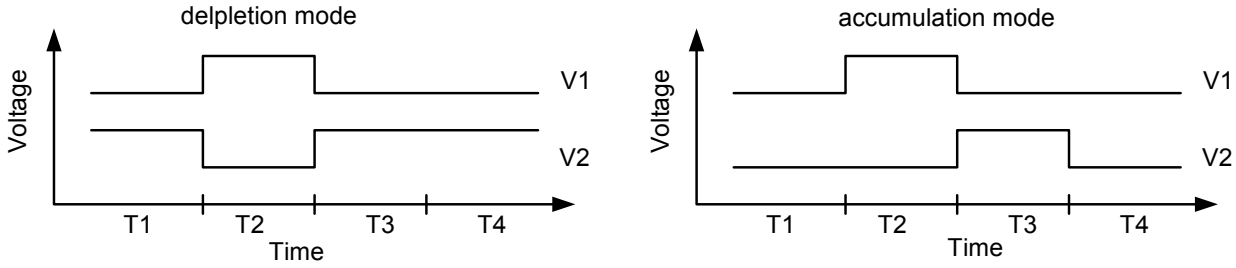

Figure 7: The timing diagrams for depletion mode (left) and accumulation mode (right) clocking.

The solution to the p-well bounce problem is to place compensating clock edges on the opposite VCCD gate. This is illustrated in Figure 8. When V1 switches to 0 V at time T2, V2 has a compensating clock edge from -9 V to -14 V. When V2 goes from -9 V to -14 V the channel potential under the gate does not change because the channel surface is pinned. The effect of going further into accumulation is it can collect the holes from the other gate switching into depletion. This stabilizes the p-well voltage and allows fast efficient charge transfer.

At time T2, the compensating clock on V2 from –9 V to –14 V is a -5 V change while the V1 clock has a +9 V change. The –5 V change is enough to collect all of the holes from the V1 gate. The capacitance of the gate when in accumulation is larger than when in depletion so the voltage change into accumulation can be smaller than the change into depletion. This keeps the low clock voltage from exceeding –15 V. The length of the time intervals T2 and T3 in Figure 8 can be as short as 1.4 µs on the KAI-4020 sensor.

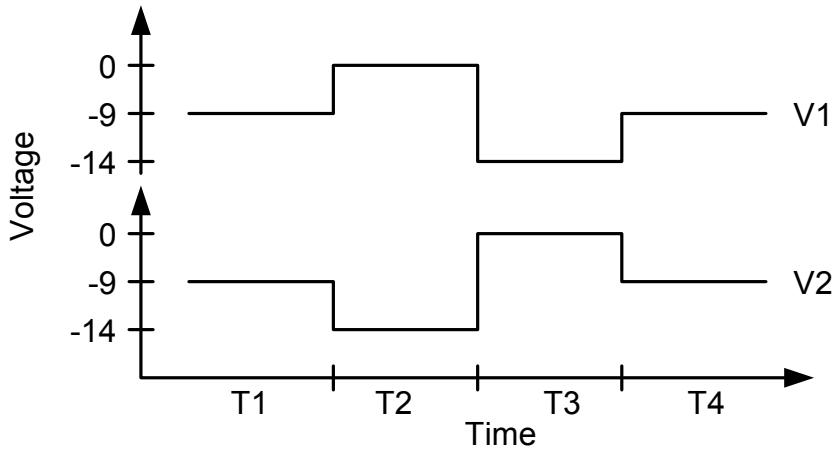

Figure 8: The new accumulation mode timing diagram for an interline CCD.

The dark current generation rate of the VCCD with accumulation mode clocking is reduced to a level comparable to the photodiode generation rate. When the generation rate drops below 20 electrons/s a new source of dark signal appears. The VCCD dark signal contains a constant (temperature independent) background signal of electrons equal to about 19 electrons. The background signal is strongly dependent on the VCCD clock pulse width and the highest voltage level of the accumulation clock waveform in Figure 8. Figure 9 shows the dependence of the background signal as a function of pulse width. The source of the background signal is spurious charge generation.[3] When a VCCD gate goes from accumulation to depletion not all holes immediately transfer to the neighboring gate. Some are trapped for a short period of time and are emitted after the gate is at its high voltage level. The high field strength between the depleted and accumulated gate causes the impact ionization of electrons as the holes move to the accumulated phase. This signal is reduced to less than 1 electron per pixel if a 32 ohm resistor is placed in series with the VCCD clock driver. This slows down the rise time of the VCCD clock driver from 100 ns to 6 µs.

Figure 10 shows the dark current generation rate of the KAI-4020 sensor with accumulation mode clocking. Now the VCCD generation rate is less than the photodiodes. For a 5 s readout time at 1 MHz and 40 C the VCCD dark current will add, on average, 6 electrons to each pixel. The accumulation mode dark current is 630 times better than depletion mode. The reduction of dark current by switching to accumulation mode will vary on the amount of spurious charge and the VCCD clock periods T2 and T3 in Figure 9. The accumulation mode dark current generation rate is not dependent on the line rate as it is for depletion mode.

The accumulation channel potential difference between the barrier implants and the CCD channel is less than in depletion. This reduces the charge capacity in accumulation mode by 5 to 10% compared with depletion mode. The charge capacity can be improved by adjusting the poly 1 and poly 2 barrier implants for unequal accumulation channel potentials. This allows charge to spill over one of the barrier implants and be stored under two gates instead of one. However, the ultimate charge handling capacity will be limited by the depletion mode charge capacity.

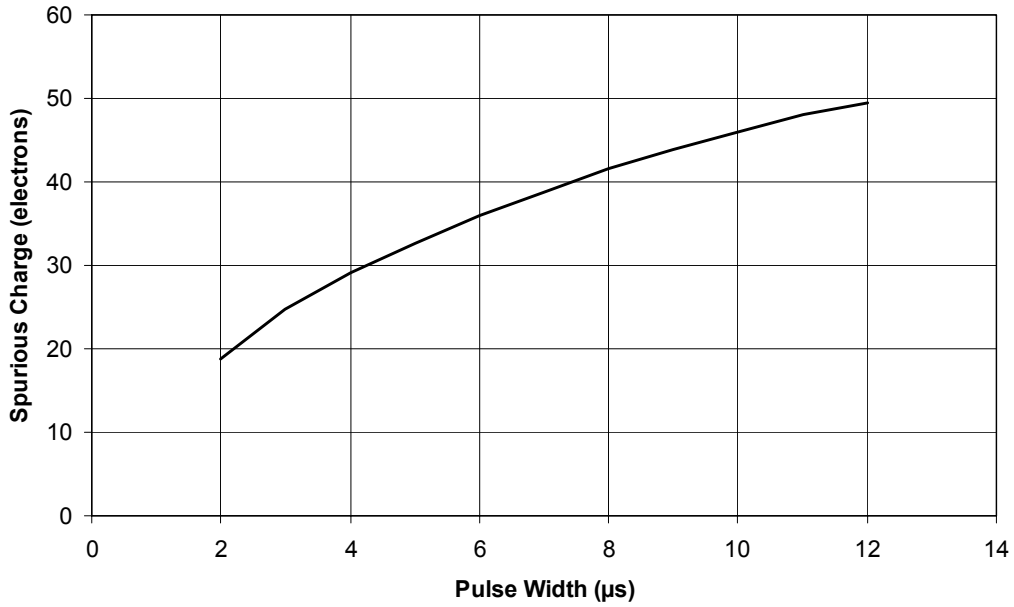

Figure 9: The spurious charge signal vs VCCD clock pulse width.

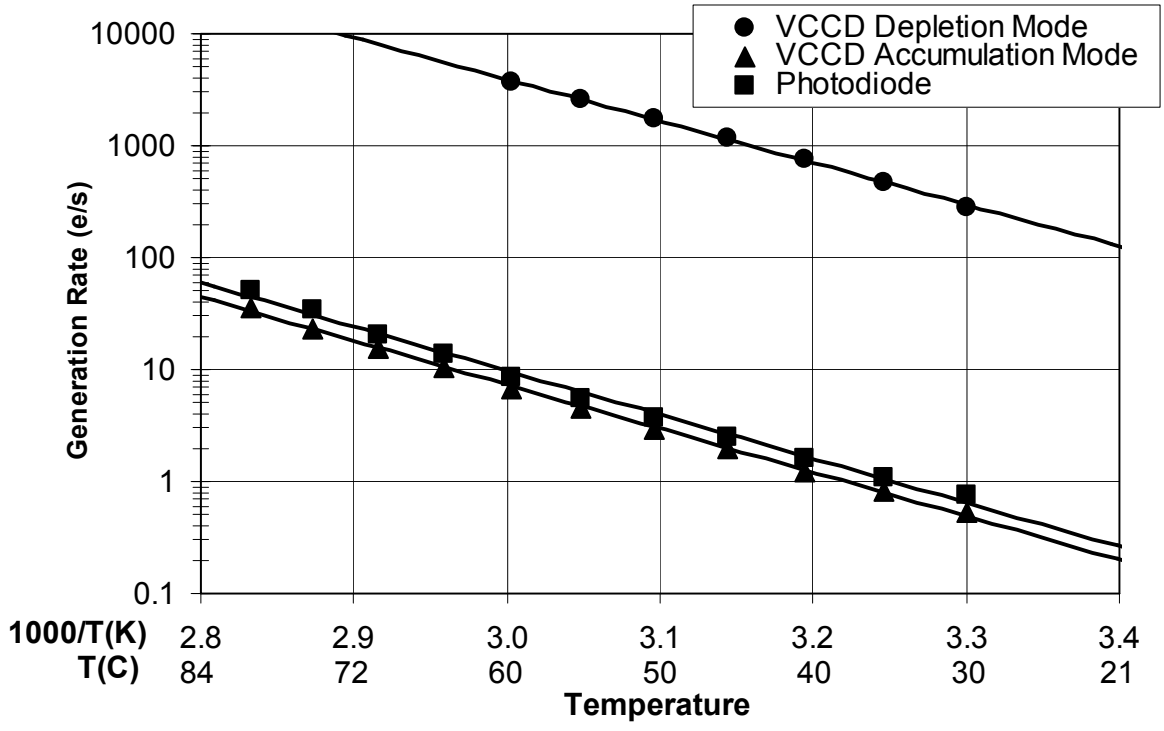

Figure 10: The dark current temperature dependence for the KAI-4020 sensor VCCD. The line rate is 416 Hz.

4. ACCUMULATION CLOCKING OF A MULTIPHASE CCD

The previous discussion was regarding two-phase CCD image sensors. Accumulation mode clocking of a 3, 4, or more phase interline CCD is also possible. As long as all VCCD clock edges are balanced there will be no p-well bounce to degrade charge transfer efficiency. When all gates are put into accumulation the channel potential under all gates will be equal. There needs to be a method of separating the charge packets. This is done by adding a barrier implant under the CCD gates. It may also be done by altering the gate dielectric thickness under the CCD gates.

The generalized clocking scheme for a 2 or more phase CCD can be described by a simple expression. Let C_n be the capacitance of phase *n* of the CCD. Let ΔV_n be the voltage change on phase *n* at a one time interval. For a stable p-well in an interline CCD, the sum of products of the capacitances and voltage changes should be near zero $\sum_n C_n \Delta V_n \cong 0$. In other words, the flow of holes into or out of the CCD p-well should be near zero. This generally requires more than 2 voltage levels on the VCCD clock driver.

Figure 11 shows the architecture and clocking scheme of a four-phase CCD. Charge packets are stored under all four phases for maximum charge capacity. Figure 12 shows the VCCD clock timing diagram. Each phase requires three voltage levels. All phases begin in the accumulated state and end in the accumulated state after shifting the charge packets one pixel.

If an additional barrier implant is put under phases V1 and V3 in Figure 11, the CCD may be clocked as a 2-phase or 4-phase CCD. For 2-phase clocking V1 and V3 would be clocked as V1, and V2 and V4 would be clocked as V2. The KAI-4020 sensor has this structure. It allows the image sensor to be imaged as a progressive scan 2-phase sensor or as an interlaced 4-phase sensor. Both modes allow for accumulation mode clocking. The advantage of the 4-phase interlaced mode is the charge capacity of the VCCD is more than double the progressive scan 2-phase charge capacity.

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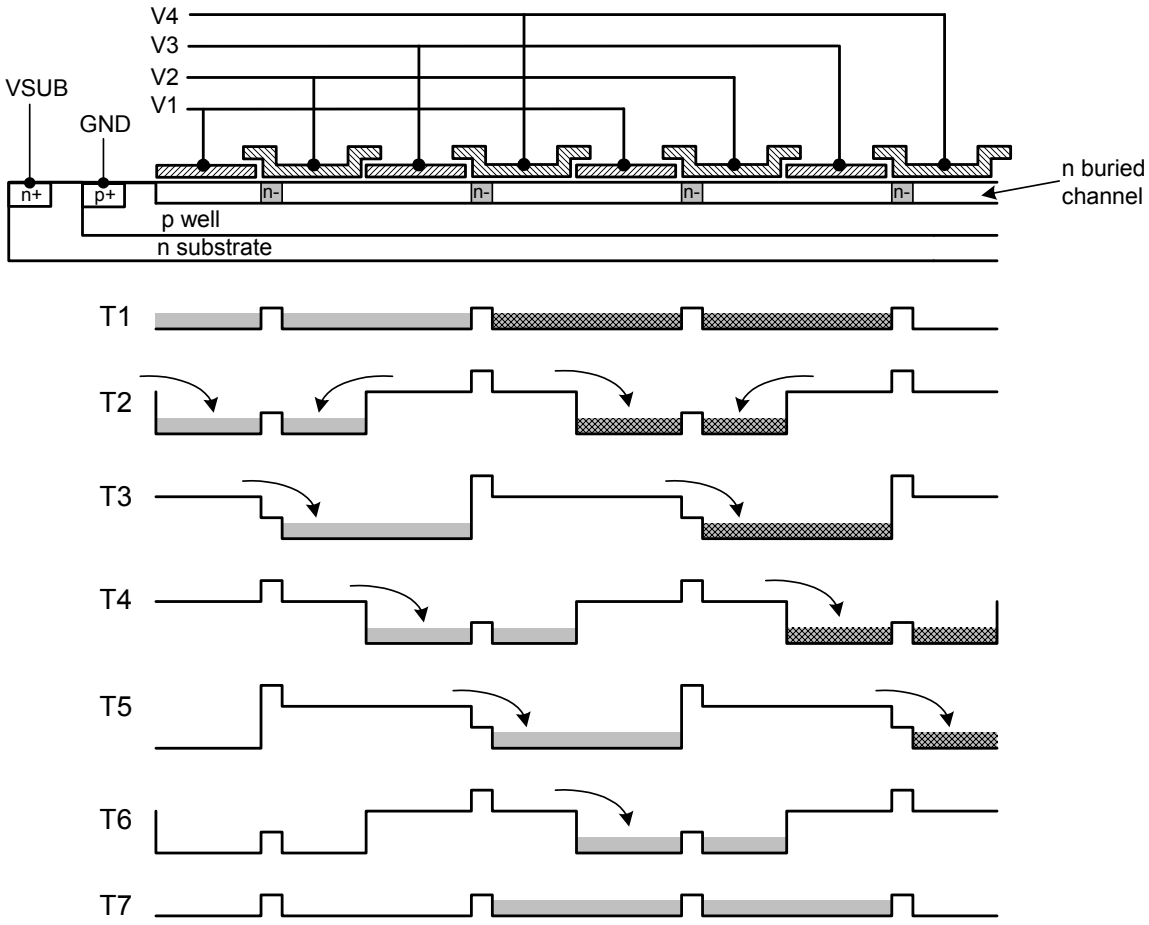

Figure 11: The 4-phase CCD accumulation mode clocking.

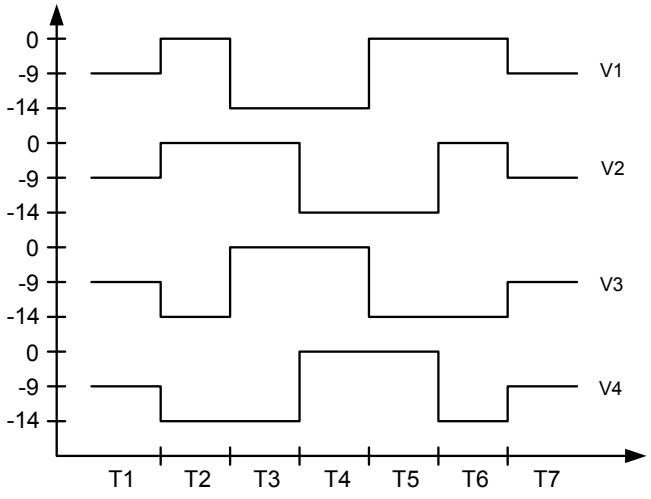

Figure 12: The 4-phase accumulation mode clock timing diagram.